

WHAT IS CLAIMED IS:

1. A semiconductor memory having a memory core for dynamically holding data, the semiconductor memory comprising:

5 a first buffer circuit for inputting an enable signal for controlling a standby state or a nonstandby state;

 a second buffer circuit for outputting a predetermined logic signal or a read/write signal for controlling the reading of data from or the writing of data to the memory core in accordance
10 with the enable signal;

 a third buffer circuit for outputting an inverted signal obtained by inverting the logic signal or the read/write signal in accordance with the enable signal;

15 a control circuit for controlling the reading or writing of the data by the logic signal or the read/write signal outputted from the second buffer circuit; and

 a data output control circuit for controlling the inputting of the data from or the outputting of the data to the outside by the inverted signal or the read/write signal
20 outputted from the third buffer circuit.

2. The semiconductor memory according to claim 1, wherein the second buffer circuit outputs the logic signal when an enable signal for controlling the standby state is being inputted.

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3. The semiconductor memory according to claim 1, wherein the second buffer circuit outputs the read/write signal when

an enable signal for controlling the nonstandby state is being inputted.

4. The semiconductor memory according to claim 1, wherein
5 the third buffer circuit outputs the inverted signal when an enable signal for controlling the standby state is being inputted.

5. The semiconductor memory according to claim 1, wherein
10 the third buffer circuit outputs the read/write signal when an enable signal for controlling the nonstandby state is being inputted.

6. The semiconductor memory according to claim 1, wherein
15 the second buffer circuit and the third buffer circuit are adjacent.

7. The semiconductor memory according to claim 1, wherein
the second buffer circuit and the third buffer circuit are
20 activated or deactivated at the same time.